GAU 1765

#3/4

PATENT

1/10/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Zheng et al.	Examiner:	Brown, C.
Serial No.:	09/437,006	Group Art Unit:	1765
Filed:	November 9, 1999	Docket No.:	VLSI.268PA
Title:	ETCH PROCESS THAT RESISTS NOTCHING AT ELECTRODE BOTTOM		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on December 21, 2000.

By: Lynda J. Bauer
Lynda J. Bauer

RESPONSE TO OFFICE ACTION

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the Office Action dated September 21, 2000, please reconsider the application in view of the following.

In The Claims

Please cancel claim 2 and amend claims 1 and 4 as follows:

1. (Amended) A process of forming a semiconductor device, comprising:

forming at least one device layer over a wafer surface;

providing a mask over a portion of the device layer; and

using a plasma-etch using first and second etching chemistries, and selectively etching into the device layer to form a pillar structure having at least one sidewall, the selective etching including use of nitrogen in an amount less than about ten percent of gas flow in a second etching chemistry, as part of the plasma etch in the second chemistry.